WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a semiconductor substrate;

a first gate electrode formed on said semiconductor substrate;

a first diffusion layer formed in said semiconductor substrate, said first diffusion layer being provided under one of opposite side portions of said first gate electrode;

a second diffusion layer formed in said semiconductor substrate, said second diffusion layer being under another one of said opposite side portions of said first gate electrode;

a second gate electrode formed on said semiconductor substrate, a side portion of the second gate electrode being provided on said second diffusion layer;

a first insulating film formed on said semiconductor substrate, said first insulating film covering said first gate electrode, said second gate electrode, said first diffusion layer and said second diffusion layer, a portion of said first insulating film being embedded between said first gate electrode and said second gate electrode, a thickness of a portion of said first insulating film, which is provided on said first diffusion layer, being thinner than a thickness of said portion of said first

insulating film, which is embedded between said first gate electrode and said second gate electrode, said first insulating film not containing nitrogen as a major component;

a second insulating film formed on said first insulating film;

an interlayer insulating film formed on said second insulating film, a major component of said interlayer insulating film being different from a major component of said second insulating film; and

a contact electrode connected to said first diffusion layer, said contact electrode being formed in said first insulating film, said second insulating film and said interlayer insulating film.

2. The semiconductor device according to claim 1, wherein a width of said first diffusion layer is larger than a width of said second diffusion layer.

3. The semiconductor device according to claim 1, wherein a density of hydrogen contained in said first insulating film is smaller than a density of hydrogen contained in said second insulating film.

4. The semiconductor device according to claim 1, wherein a density of trap with respect to electric charge existing in said first insulating film is smaller than a density of trap with respect to electric charge existing in said second insulating film.

5. The semiconductor device according to claim 1,

wherein said first insulating film is made of a material selected from a group including silicon oxide, oxy-nitride and oxidized silicon nitride.

6. The semiconductor device according to claim 1, wherein said second insulating film is made of silicon nitride.

7. The semiconductor device according to claim 1, wherein a void is provided between said first gate electrode and said second gate electrode.

8. The semiconductor device according to claim 1, wherein said portion of said first insulating film is embedded between said first gate electrode and said second gate electrode to a height equal to a height of said first gate electrode and said second gate electrode.

9. The semiconductor device according to claim 1, wherein said portion of said first insulating film is embedded between said first gate electrode and said second gate electrode to a height in a middle of a height of said first gate electrode and said second gate electrode.

10. The semiconductor device according to claim 1, wherein said portion of said first insulating film is provided on side surfaces of said first gate electrode and said second gate electrode.

11. The semiconductor device according to claim 1, wherein a further portion of said first insulating film

is formed on upper surfaces of said first gate electrode and said second gate electrode.

12. The semiconductor device according to claim 1, wherein said contact electrode is formed in a self-align manner to said first gate electrode.

13. A semiconductor device comprising:

a semiconductor substrate;

a plurality of memory cell gates formed on said semiconductor substrate;

a selecting gate formed on said semiconductor substrate, said selecting gate being adjacent to said plurality of memory cell gates and functioning to control said plurality of memory cell gates;

a diffusion layer formed in said semiconductor substrate, said diffusion layer being provided under a side portion of said selecting gate which is opposite to another side portion of said selecting gate which is adjacent to said memory cell gates;

a first insulating film formed on said semiconductor substrate, said first insulating film covering said memory cell gates, said selecting gate and said diffusion layer, portions of said first insulating film being embedded between said memory cell gates, another portion of said first insulating film being embedded between an outermost one of said memory cell gates and said selecting gate, said first insulating film not containing nitrogen as a major

component;

a second insulating film formed on said first insulating film;

an interlayer insulating film formed on said second insulating film, a major component of said interlayer insulating film being different from a major component of said second insulating film; and

a contact electrode connected to said diffusion layer, said contact electrode being formed in said first insulating film, said second insulating film and said interlayer insulating film.

14. The semiconductor device according to claim 13, wherein a thickness of said portions of said first insulating film, which are embedded between said memory cell gates, is thicker than a thickness of a further portion of said first insulating film, which is on said first diffusion layer.

15. The semiconductor device according to claim 13, wherein a thickness of a portion of said first insulating film, which is provided on said side surface of said selecting gate, is larger than half a distance between said memory cell gates.

16. The semiconductor device according to claim 13, wherein a density of hydrogen contained in said first insulating film is smaller than a density of hydrogen contained in said second insulating film.

17. The semiconductor device according to

claim 13, wherein a density of trap with respect to electric charge existing in said first insulating film is smaller than a density of trap with respect to electric charge existing in said second insulating film.

18. The semiconductor device according to claim 13, wherein said first insulating film is made of a material selected from a group including silicon oxide, oxy-nitride and oxidized silicon nitride.

19. The semiconductor device according to claim 13, wherein said second insulating film is made of silicon nitride.

20. The semiconductor device according to claim 13, wherein a void is provided in at least one between said memory cell gates.

21. The semiconductor device according to claim 13, wherein a void is provided in every between said memory cell gates.

22. The semiconductor device according to claim 13, wherein a void is provided in between an outermost one of said memory cell gates and said selecting gate.

23. The semiconductor device according to claim 13, wherein a void is provided in every between an outermost one of said memory cell gates and in between an outermost one of said memory cell gates and said selecting gate.

24. The semiconductor device according to claim 13, wherein said portions of said first insulating film are embedded to a height equal to a height of said memory cell gates, said another portion of said first insulating film is embedded to a height equal to a height of said selecting gate, and said height of said portions of said first insulating film is equal to said height of said another portion of said first insulating film.

25. The semiconductor device according to claim 13, wherein said portions of said first insulating film are embedded to a height in a middle of a height of said memory cell gates, said another portion of said first insulating film is embedded to a height in a middle of a height of said selecting gate, and said height of said portions of said first insulating film is equal to said height of said another portion of said first insulating film.

26. The semiconductor device according to claim 13, wherein said portions of said first insulating film are provided on side surfaces of said memory cell gates and said another portion of said first insulating film is formed on a side surface of said outermost one of said memory cell gates and a side surface of said selecting gate.

27. The semiconductor device according to claim 13, wherein a further portion of said first

insulating film is formed on upper surfaces of said memory cell gates and an upper surface of said selecting gate.

28. The semiconductor device according to claim 13, wherein said contact electrode is formed in a self-align manner to said selecting gate.

29. A semiconductor device comprising:

a semiconductor substrate;

a diffusion layer formed in said semiconductor substrate;

a first memory cell array including a plurality of memory cell transistors and a selecting transistor, said memory cell transistors and said selecting transistor being formed on said semiconductor substrate, said memory cell transistors each having a memory cell gate and said selecting transistor having a selecting gate, a side portion of said selecting gate being provided on said diffusion layer;

a second memory cell array including a plurality of memory cell transistors and a selecting transistor, said memory cell transistors and said selecting transistor being formed on said semiconductor substrate, said memory cell transistors each having a memory cell gate and said selecting transistor having a selecting gate, a side portion of said selecting gate being provided on said diffusion layer;

a first insulating film formed on said

semiconductor substrate, said first insulating film covering said memory cell gates of said first and second memory cell arrays, said selecting gates of said first and second memory cell arrays and said first diffusion layer, portions of said first insulating film being embedded between said memory cell gates of said first and second memory cell arrays, another portion of said first insulating film being formed between said first and second memory cell arrays, a thickness of said another portion of said first insulating film, being thinner than a thickness of said portions of said first insulating film, which are embedded between said memory cell gates, said first insulating film not containing nitrogen as a major component;

a second insulating film formed on said first insulating film;

an interlayer insulating film formed on said second insulating film, a major component of said interlayer insulating film being different from a major component of said second insulating film; and

a contact electrode connected to a portion of said first diffusion layer, which is between said first memory cell array and said second cell array, said contact electrode being formed in said first insulating film, said second insulating film and said interlayer insulating film.

30. The semiconductor device according to

claim 29, wherein a distance between said memory cell gate of said memory cell transistor of said first memory cell array and said memory cell gate of said memory cell transistor of said second memory cell array is smaller than a distance between said selecting gate of said selecting gate transistor of said first memory cell array and said selecting gate of said selecting gate transistor of said second memory cell array.

31. The semiconductor device according to claim 29, wherein a density of hydrogen contained in said first insulating film is smaller than a density of hydrogen contained in said second insulating film.

32. The semiconductor device according to claim 29, wherein a density of trap with respect to electric charge existing in said first insulating film is smaller than a density of trap with respect to electric charge existing in said second insulating film.

33. The semiconductor device according to claim 29, wherein said first insulating film is made of a material selected from a group including silicon oxide, oxy-nitride and oxidized silicon nitride.

34. The semiconductor device according to claim 29, wherein said second insulating film is made of silicon nitride.

35. The semiconductor device according to claim 29, wherein a void is provided in at least one

between said memory cell gates.

36. The semiconductor device according to claim 29, wherein a void is provided in every between said memory cell gates.

37. The semiconductor device according to claim 29, wherein a void is provided in between an outermost of said memory cell gates and said selecting gate.

38. The semiconductor device according to claim 29, wherein a void is provided in every between said memory cell gates and in between an outermost of said memory cell gates and said selecting gate.

39. The semiconductor device according to claim 29, wherein said portions of said first insulating film are embedded to a height equal to a height of said memory cell gates, said another portion of said first insulating film is embedded to a height equal to a height of said selecting gate, and said height of said portions of said first insulating film is equal to said height of said another portion of said first insulating film.

40. The semiconductor device according to claim 29, wherein said portions of said first insulating film are embedded to a height in a middle of a height of said memory cell gates, said another portion of said first insulating film is embedded to a height in a middle of a height of said selecting gate,

and said height of said portions of said first insulating film is equal to said height of said another portion of said first insulating film.

41. The semiconductor device according to claim 29, wherein said portions of said first insulating film are provided on side surfaces of said memory cell gates and said another portion of said first insulating film is formed on a side surface of said outermost one of said memory cell gates and a side surface of said selecting gate.

42. The semiconductor device according to claim 29, wherein a further portion of said first insulating film is formed on upper surfaces of said memory cell gates of said first memory cell array and an upper surface of said selecting gate of said first memory cell array and on upper surfaces of said memory cell gates of said second memory cell array and an upper surface of said selecting gate of said second memory cell array.

43. The semiconductor device according to claim 29, wherein said contact electrode is formed in a self-align manner to said selecting gates of said first and second memory cell arrays.

44. A semiconductor device comprising:

a semiconductor substrate;

a first gate electrode formed on said semiconductor substrate;

a first diffusion layer formed in said semiconductor substrate, said first diffusion layer being provided under one of opposite side portions of said first gate electrode;

a second diffusion layer formed in said semiconductor substrate, said second diffusion layer being under another of said opposite side portions of said first gate electrode;

a second gate electrode formed on said semiconductor substrate, a side portion of the second gate electrode being provided on said second diffusion layer;

a first insulating film formed on said semiconductor substrate, said first insulating film covering side surfaces of said first gate electrode, side surfaces of said second gate electrode, said first diffusion layer and said second diffusion layer, a portion of said first insulating film being embedded between said first gate electrode and said second gate electrode, a thickness of a portion of said first insulating film, which is provided on said first diffusion layer, being thinner than a thickness of said portion of said first insulating film, which is embedded between said first gate electrode and said second gate electrode, said first insulating film not containing nitrogen as a major component;

a second insulating film formed on said first

insulating film, an upper surface of said first gate electrode, an upper surface of said second gate electrode;

an interlayer insulating film formed on said second insulating film, a major component of said interlayer insulating film being different from a major component of said second insulating film; and

a contact electrode connected to said first diffusion layer, said contact electrode being formed in said first insulating film, said second insulating film and said interlayer insulating film.

45. A semiconductor device comprising:

a semiconductor substrate;

a plurality of memory cell gates formed on said semiconductor substrate;

a selecting gate formed on said semiconductor substrate, said selecting gate being adjacent to said plurality of memory cell gates and functioning to control said plurality of memory cell gates;

a diffusion layer formed in said semiconductor substrate, said diffusion layer being under a side portion of said selecting gate which is opposite to another side portion of said selecting gate which is adjacent to said memory cell gates;

a first insulating film formed on said semiconductor substrate, said first insulating film covering side surfaces of said memory cell gates, side

surfaces of said selecting gate and said diffusion layer, portions of said first insulating film being embedded between said memory cell gates, another portion of said first insulating film being embedded between said memory cell gates and said selecting gate, said first insulating film not containing nitrogen as a major component;

a second insulating film formed on said first insulating film, upper surfaces of said memory cell gates and an upper surface of said selecting gate;

an interlayer insulating film formed on said second insulating film, a major component of said interlayer insulating film being different from a major component of said second insulating film; and

a contact electrode connected to said diffusion layer, said contact electrode being formed in said first insulating film, said second insulating film and said interlayer insulating film.

46. A semiconductor device comprising:

a semiconductor substrate;

a diffusion layer formed in said semiconductor substrate;

a first memory cell array including a plurality of memory cell transistors and a selecting transistor, said memory cell transistors and said selecting transistor being formed on said semiconductor substrate, said memory cell transistors each having a

memory cell gate and said selecting transistor having a selecting gate, a side portion of said selecting gate being provided on said diffusion layer;

a second memory cell array including a plurality of memory cell transistors and a selecting transistor, said memory cell transistors and said selecting transistor being formed on said semiconductor substrate, said memory cell transistors each having a memory cell gate and said selecting transistor having a selecting gate, a side portion of said selecting gate being provided on said diffusion layer;

a first insulating film formed on said semiconductor substrate, said first insulating film covering side surfaces of said memory cell gates of said first and second memory cell arrays, side surfaces of said selecting gates of said first and second memory cell arrays and said first diffusion layer, portions of said first insulating film being embedded between said memory cell gates of said first and second memory cell arrays, another portion of said first insulating film being formed between said first and second memory cell arrays, a thickness of said another portion of said first insulating film, being thinner than a thickness of said portions of said first insulating film, which are embedded between said memory cell gates, said first insulating film not containing nitrogen as a major component;

a second insulating film formed on said first insulating film, upper surfaces of said memory cell gates of said first and second memory cell arrays and upper surfaces of said selecting gates of said first and second memory cell arrays;

an interlayer insulating film formed on said second insulating film, a major component of said interlayer insulating film being different from a major component of said second insulating film; and

a contact electrode connected to a portion of said first diffusion layer, which is between said first memory cell array and said second cell array, said contact electrode being formed in said first insulating film, said second insulating film and said interlayer insulating film.

47. A method of manufacturing a semiconductor device comprising:

forming a first gate electrode and a second gate electrode on a semiconductor substrate;

forming a diffusion layer, with the first gate electrode as a mask

forming a first insulating film not containing nitrogen as a major component on said semiconductor substrate to cover said first gate electrode, said second gate electrode and said diffusion layer in such a manner that a portion of said first insulating film is embedded between said first gate electrode and said

second gate electrode to a height equal to a height of said first gate electrode or above, another portion of said first insulating film is provided on a major part of said diffusion layer to a height lower than a height of said first gate electrode and a further portion of said first insulating film is provided on a minor part of said diffusion layer to a height equal to a height of said first gate electrode or above;

forming a second insulating film on said first insulating film;

forming on said second insulating film an interlayer insulating film whose etching rate is larger than an etching rate of said second insulating film;

etching a portion of said first insulating film, a portion of said second insulating film and a portion of said interlayer insulating film, which are on said major part of said diffusion layer, to form a contact hole leading to said major part of said diffusion layer; and

embedding a conductive material in said contact hole to form a contact electrode connected to said major part of said diffusion layer.

48. A method of manufacturing a semiconductor device comprising:

forming, on a semiconductor substrate, a plurality of first memory cell gates, a pair of first selecting gates sandwiching said first memory cell gates, a

plurality of second memory cell gates and a pair of second selecting gates sandwiching said second memory cell gates;

forming a plurality of diffusion layers in said semiconductor substrate while using as masks said first memory cell gates, said pair of first selecting gates, said second memory cell gates and said pair of second selecting gates;

forming a first insulating film not containing nitrogen as a major component on said semiconductor substrate to cover said first memory cell gates, said second memory cell gates and said diffusion layers in such a manner that portions of said first insulating film are embedded between said first memory cell gates and between said second memory cell gates, a portion of said first insulating film is provided on one of said diffusion layers, on which one of said pair of first selecting gates is adjacent to one of said pair of second selecting gates in such a manner that a part of said portion of said first insulating film, which is on a major part of said one of said diffusion layers, has a thickness thinner than a thickness of said portions of said first insulating film, which are embedded between said first memory cell gates and between said second memory cell gates;

forming a second insulating film on said first insulating film;

forming on said second insulating film an interlayer insulating film whose etching rate is larger than an etching rate of said second insulating film;

etching a portion of said first insulating film, a portion of said second insulating film and a portion of said interlayer insulating film, which are on said major part of said one of said diffusion layers, to form a contact hole leading to said major part of said one of said diffusion layers; and

embedding a conductive material in said contact hole to form a contact electrode connected to said major part of said one of said diffusion layers.